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Patent
Avago Technologies Docket No.: 10004400-1

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application of: Benny W. H. Lai
Application No.: 10/068,326
Filed: February 6, 2002

Group Art Unit: 2138
Examiner: Tabone Jr., John J.
Docket No.: 10004400-1
Confirmation No.: 8823

For: **EMBEDDED TESTING CAPABILITY FOR INTEGRATED SERIALIZER/DESERIALIZERS**

DECLARATION OF BENNY W. H. LAI UNDER 37 C.F.R. §1.131

Mail Stop Amendment
Commissioner of Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SMITH FROHWEIN TEMPEL
GREENLEE BLAHA LLC
CUSTOMER NO. 35856

Sir:

I, Benny W. H. Lai, state the following:

1. I am the inventor of the subject matter disclosed, and claimed, in the above-referenced patent application.
2. The invention of the above-referenced patent application was conceived at least as early as August 16, 2001, as evidenced by the Agilent Technologies Invention Disclosure Form, assigned PDNO No. 10004400, a true and accurate copy of which is attached hereto as Exhibit A (date redacted). From at least as early as August 16, 2001, I diligently pursued the preparation of a U.S. Utility Patent application. Prior to August 16, 2001, the invention disclosure was submitted in accordance with Agilent Technologies' corporate procedures. During the time from prior to August 16, 2001, to February 6, 2002, I continued to develop the invention as permitted given my usual workload, which included assisting in the preparation of many U.S. patent applications. I diligently assisted in the preparation of the above-identified U.S. patent application, the filing of

which constitutes a constructive reduction to practice of the subject matter disclosed, and claimed, in the above-referenced patent application.

3. The invention was built and tested, as evidenced on page 1 of the Agilent Technologies Invention Disclosure Form, PDNO No. 10004400 (date redacted) prior to August 16, 2001. The construction and testing of the invention constitutes an actual reduction to practice of the invention prior to August 16, 2001.

4. Based on the description of the system and method for testing of embedded SERDES as detailed in the Agilent Technologies Invention Disclosure Form, PDNO No. 10004400, a person having ordinary skill in the art would be possessed of sufficient information to practice the invention at least as early as August 16, 2001, and would consider the invention to be actually reduced to practice prior to August 16, 2001 and constructively reduced to practice no later than February 6, 2002.

I HEREBY DECLARE that all statements made herein of my own knowledge are true, and that all statements made on information and belief are believed to be true, and that these statements are made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code, and that any such willful false statements may jeopardize the validity of the above-referenced patent application, or any patent issued thereon.

Benny W. H. Lai

Benny W. H. Lai

July 28, 2006

Date

CERTIFICATE OF FACSIMILE TRANSMISSION UNDER 37 C.F.R. § 1.8

I hereby certify that this correspondence, including any items indicated as attached or included, is being transmitted via facsimile transmission to the United States Patent and Trademark Office, (571) 273-8300, on the date indicated below.

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8/1/6

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EXHIBIT A

Agilent Technologies

INVENTION DISCLOSURE

PDNO 1000 4400 DATE RCVD ATTORNEY JCP PAGE ONE OF 1/10 ICBD

Instructions: The information contained in this document is COMPANY CONFIDENTIAL and may not be disclosed to others without prior authorization. Submit this disclosure to the Agilent Technologies Legal Department as soon as possible. No patent protection is possible until a patent application is authorized, prepared, and submitted to the Government.

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Descriptive Title of Invention:

Method for Dynamic Testing of Embedded SerDes

Name of Project: QTA ("Q" test asic): embedded SerDes demostration for Cisco under NDA

Product Name or Number:

Was a description of the invention published, or are you planning to publish? If so, the date(s) and publication(s):

no

Was a product including the invention announced, offered for sale, sold, or is such activity proposed? If so, the date(s) and location(s):

no

Was the invention disclosed to anyone outside of AGILENT TECHNOLOGIES, or will such disclosure occur? If so, the date(s) and name(s):

no

If any of the above situations will occur within 3 months, call your IP attorney or the Legal Department now at 1-553-3061 or 408-553-3061.

Was the invention described in a lab book or other record? If so, please identify (lab book #, etc.)

computer files, intranet, note book "Captone Evaluation"

Was the invention built or tested? If so, the date:

tested

Was this invention made under a government contract? If so, the agency and contract number:

no

Description of Invention: *Please preserve all records of the invention and attach additional pages for the following. Each additional page should be signed and dated by the inventor(s) and witness(es).*

A. Prior solutions and their disadvantages (if available, attach copies of product literature, technical articles, patents, etc.).
B. Problems solved by the invention.
C. Advantages of the invention over what has been done before.
D. Description of the construction and operation of the invention (include appropriate schematic, block, & timing diagrams; drawings; samples; graphs; flowcharts; computer listings; test results; etc.)

Signature of Inventor(s): Pursuant to my (our) employment agreement, I (we) submit this disclosure on this date: 01/00/7129

Employee No.	Name	Signature	Telnet	Mailstop	Entity & Lab Name
229012	Benny W.H. Lai	Benny W.H. Lai	435-4299	90-UA	ICBD / HSLO

(If more than four inventors, include additional information on another copy of this form and attach to this document)

PAGE 12/21 * RCVD AT 8/1/2006 4:10:22 PM [Eastern Daylight Time] * SVR:USPTO-EFXRF-5/12 * DNIS:2738300 * CSID:7708040900 * DURATION (mm-ss):04-54

S1 INVENTION DISCLOSURE COMPANY CONFIDENTIAL PAGE 2 OF 10

Signature of Witness(es): *(Please try to obtain the signature of the person(s) to whom invention was first disclosed.)*
The invention was first explained to, and understood by, me (us) on this date: [ ]

Full Name	Signature	Date of Signature
Ralph E. Lovelace	Ralph E. Lovelace	/ /
CHARLES WANG	Charles Wang	/ /

Inventor & Home Address Information: *(If more than four inventors, include addt'l information on a copy of this form & attach to this document)*

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Method for Dyn. .ic Testing of Embedded Ser.es

Benny Lai

With the recent growth in networking, the demand for faster and cheaper systems have driven the level of integration of components higher and higher. One such element is the Serializer/Deserializer (SerDes) function. In prior years, these functions were on separate chips. As circuits techniques and processes improved, these two functions were integrated into a single die (the first SerDes). Recently, dies containing four SerDes have become available.

The SerDes's serializer function is to take a parallel data word (typically encoded with 8b/10b) and multiplexes them into a serial data stream at 10 times the parallel rate. The serializer function is often referred as the transmitter, or Tx. The deserializer portion, often referred to as the the receiver, or Rx, takes in this data stream and recovers the original 10 bits at its parallel output. Implementation of the SerDes function require clock generation and clock and data recovery. These have been traditionally implemented with Phase-Lock-Loops and other analog circuit techniques.

A major application with SerDes functional blocks is the switch fabric, where a VLSI switch logic chip is interfaced to multiple SerDes IC's. The parallel interface of the SerDes IC's are connected to the switch logic chip. The need to reduce the chip count and board space is the motivation behind the integration of multiple SerDes.

The next step in SerDes integration is to embed the SerDes directly into the switch logic chip itself. This integration not only removes the discrete SerDes blocks, it also removes the many parallel data lines which interfaces the switch logic chip and the SerDes chips, in turn conserving board space, and drastically reducing power.

Testing Limitations of Embedded SerDes

Discrete SerDes are tested at the specified speed to insure proper functionality. The parallel data at the Tx input is dynamically toggled, and the recovered data at the Rx is compared to the data transmitted. These test are carried out over the various modes such as loop-back and byte-sync enable. A functional test at the spec speed insures the signal integrity of the output drivers, and the subtle behaviors of the PLL's are all tested.

The stimulus and measurements of the parallel data at the Tx and Rx of the SerDes is performed with high-speed IC test systems. One test system is the Bit-Error-Rate Tester (BERT). This machine generates pseudo random bit sequence (PRBS) patterns and continuously monitor the received PRBS pattern for errors in the transmission. Since acceptable error rates in network systems is typically below 1e-9, over a billion bits must be passed before a single error occurs. The BERT monitors these errors and records the bit error rate.

Since the parallel signals which interface between the embedded SerDes and the switch logic core are now internal to the IC, the traditional methods of SerDes testing cannot be used. Thus

multiple embedded SerDes within an IC needs to be developed.

Furthermore, as the SerDes's analog functions are sensitive to crosstalk and supply variations, functionality of a single embedded SerDes channel does not insure that it will be properly working with multiple channels turned on. The test needs to be performed with all SerDes running simultaneously.

The reqirements for this test system are:

1. control the Tx parallel data and modes at each SerDes.
2. measure the parallel data and status at each Rx of the SerDes.
3. perform functional tests at the specified speed for each SerDes.

   To simulate a real environment, a PRBS pattern is needed. The BER performance needs to be monitored continuously. Also this test should be run concurrently for all embedded SerDes, making the effects such as cross-talk and supply variation as realistic as possible.

Invention Description

This invention is designed to overcome the testing limitations of embedded SerDes. The block diagram is show in figure 1. It consists of three major functional blocks: the functional test controller (FTC), functional test interface (FTI) and the In/Out Controller (IOC). A auxiliary block of Built-In Self-Test (BIST) can be added to the test bus for automated testing. These functional blocks all communicate via a test bus, which include the address, commands, and data.

An FTI block is a fitted between each SerDes and the logic core. This block intercepts the parallel data going in either direction, and can perform the functions of loop-back, static data testing, and dynamic data testing with a PRBS generator and error detector. The modes of the FTI block, as well as the embedded serdes block, are controlled by a dedicated FTC block. This block is assigned an address, similar to Ethernet. A common test bus is shared amongst all FTC blocks. The address, control instructions, and data are transmitted onto this test bus to all FTC blocks by the IOC. Commands and address are interpreted by the FTC block, and in turn controls the FTI. The IOC block is an interface to the outside world; in this embodiment, this is translated to an RS232 interface, allowing access through a serial port of a Personal Computer. The test bus can also be accessed by BIST state machine.

This common bus structure allows a PC to have easy access to the parallel signals of the SerDes, fulfilling requirements 1 and 2. This test structure alone can also perform static data testing; that is, static data can be set at each of the parallel Tx inputs of each SerDes, and with the loop-back mode engaged, the expected bits at the Rx parallel data can be compared. This test can pin-point gross processing defects such as metal shorts.

To gain full functional test at speed (requirement #3), a 2^7-1 PRBS generator and an error detector receiver are built into the FTI block. The 2^7-1 sequence is traditionally generated at the serial rate with 7 flip-flops and one Xor gate, as shown in figure 2. Since we require a 10-bit pattern to be fed into the Tx parallel input, one could take the output of the 7 flip-flop PRBS generator, and demultiplex it 1 to 10. This method of a 10 bit parallel 2^7-1 generation is

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intensive as the 7 flip-flops, as well as the demux, are running at the very fast serial rate.

A more direct method of generating the equivalent 10 bits is shown in figure 3. Here, the 10 bits are generated at the parallel rate, such that when the 10 bits are serialized, the resulting data stream is the required 2^7-1 pattern. The state equations for this circuit is shown in table 1.

One method of PRBS error detection is to directly compare the received bits to the transmitted bits. However, since the test may include an unknown length of cable, the delay of the pattern cannot be determined. This direct comparison is thus impractical.

To overcome this, the receiver has an independent 10-bit PRBS generator identical to that of the transmitter. Since the bit sequence is derived from know states, the received parallel data is simply seeded onto the pattern generator. During the seeding process, it is assumed that the 10 bit loaded are error-free. This is valid since one error in 10 consecutive bit is extremely low when the BER is below one in one billion. The errors are then counted and stored in a local register within the FTI. This value can then be polled from the PC through the IOC.

Our embodiment of the integrated BER tester also include common patterns such as a toggling pattern of 1010101010 and 1100110011 and their compliments. These toggling patterns can expose weaknesses of the SerDes due to the induced power supply variations.

Advantages of Present Invention

With this testing system, all embedded SerDes blocks can be addressed, controlled, and monitored independently. For example, for a VLSI chip with multiple embedded SerDes, each be controlled for the desired mode, such as loop-back, power-down etc. The normal functions of BIST using static data to test each SerDes can pinpoint processing defects. In addition, since each SerDes has its own built-in PRBS pattern generator and error detector, the entire chip can be exercised at it nominal operating bit rate. This system allows all the SerDes to be operating simultaneously while each SerDes's BER is monitored.

Another advantage of this self-seeding error detection method is the ability to synchronize to an external PRBS pattern unrelated to the Tx of the SerDes. For example, this PRBS pattern can be generated with an external BERT or other chips with embedded SerDes.

Preferred Embodiment and Proposed Claims

The following is a list of the contributions of this patent which needs to be captured in the final claims. The order below may not be optimal legally.

1. System of Embedded SerDes testing consisting of:

    a. a Functional Test Interface (FTI) which is inserted between the parallel signals between the SerDes and the logic core

    b. a Functional Test Controller (FTC) which interprets the commands on the shared test bus, and sets the modes of the SerDes and FTI. Each FTC is assigned an address.

c. a Input/Output Controller (IOC) which interfaces the test bus to the external world such as with a RS232 serial port. 6/10

d. a Built-In-Self-Test (BIST) state machine which connects to the test bus, and controls the self-test sequence.

e. a shared test bus containing address, command and data, is shared to each FTI, the IOC and the BIST blocks

2. The FTI consists of

a. a through mode where parallel data is passed through from the core to the SerDes. This is the normal mode.

b. a loop-back mode where the parallel Rx outputs of the SerDes is wrappe back to the Tx parallel inputs. This is often is "serial loop-back", since the serial data from the Rx high-speed input is transmitter back out at the Tx serial high-speed output.

c. a test mode where a static or dynamic pattern set is injected at the Tx parallel input. The pattern is clocked at the parallel rate.

d. a test mode where the dynamic pattern is a 2^7-1 PRBS pattern.

g. a test mode where the parallel output of the SerDes is detected and compared to a pattern set. The error discrepancies are counted and stored; and can be retrieve with a command from the FTC.

3. The FTI pattern set includes a 2^7-1 PRBS generator consists of

a. state equations and schematic described in figures 3ab.

4. The FTI error detection includes a 2^7-1 PRBS receiver consisting of

a. the PRBS generator as described in claim 3, and seeded with the SerDes's Rx parallel output.

b. a method to compare the subsequent Rx parallel outputs with those predicted with the seeded PRBS generator.

c. a counter to store the bit discrepancies.

5. The IOC consists of

a. means to interface to the test bus, and an external bus such as RS232 serial protocol.

6. The BIST (built-in self test) state machine consisting of:

a. access and control to the test bus

b. states for functional and parametric testing

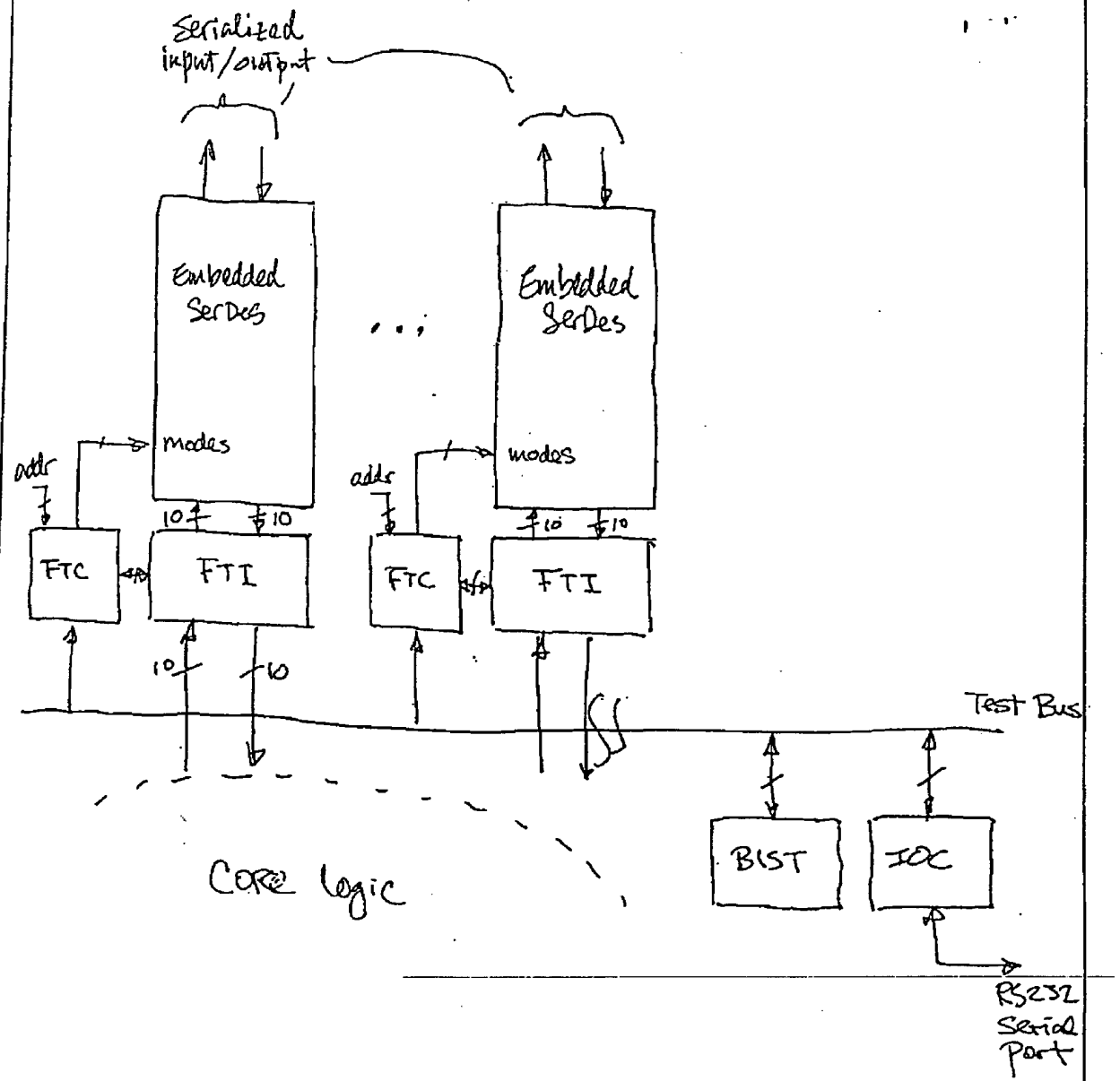

figure 1. Access & Testing of the Embedded SerDes are accomplished with the FTI, FTC, IOC, & BIST blocks, which communicate via a common test bus.

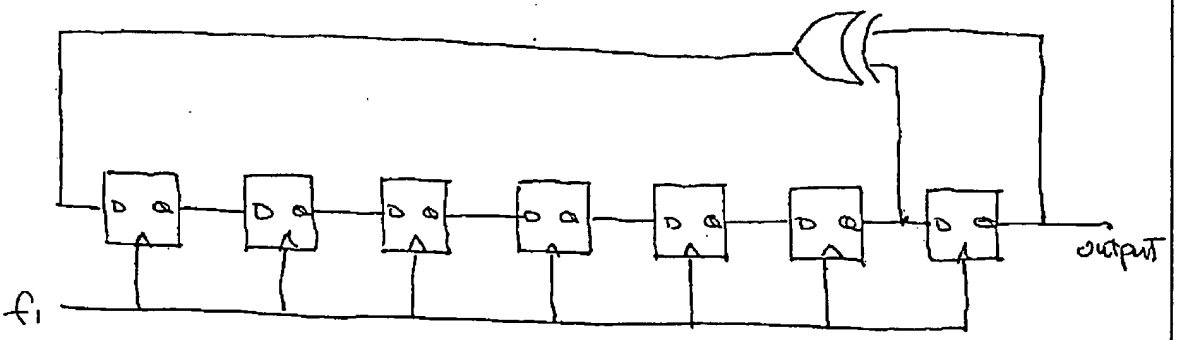

figure 2 Traditional PRBS 2^7-1 pattern generator, clocking at the high speed clock rate (f_1)

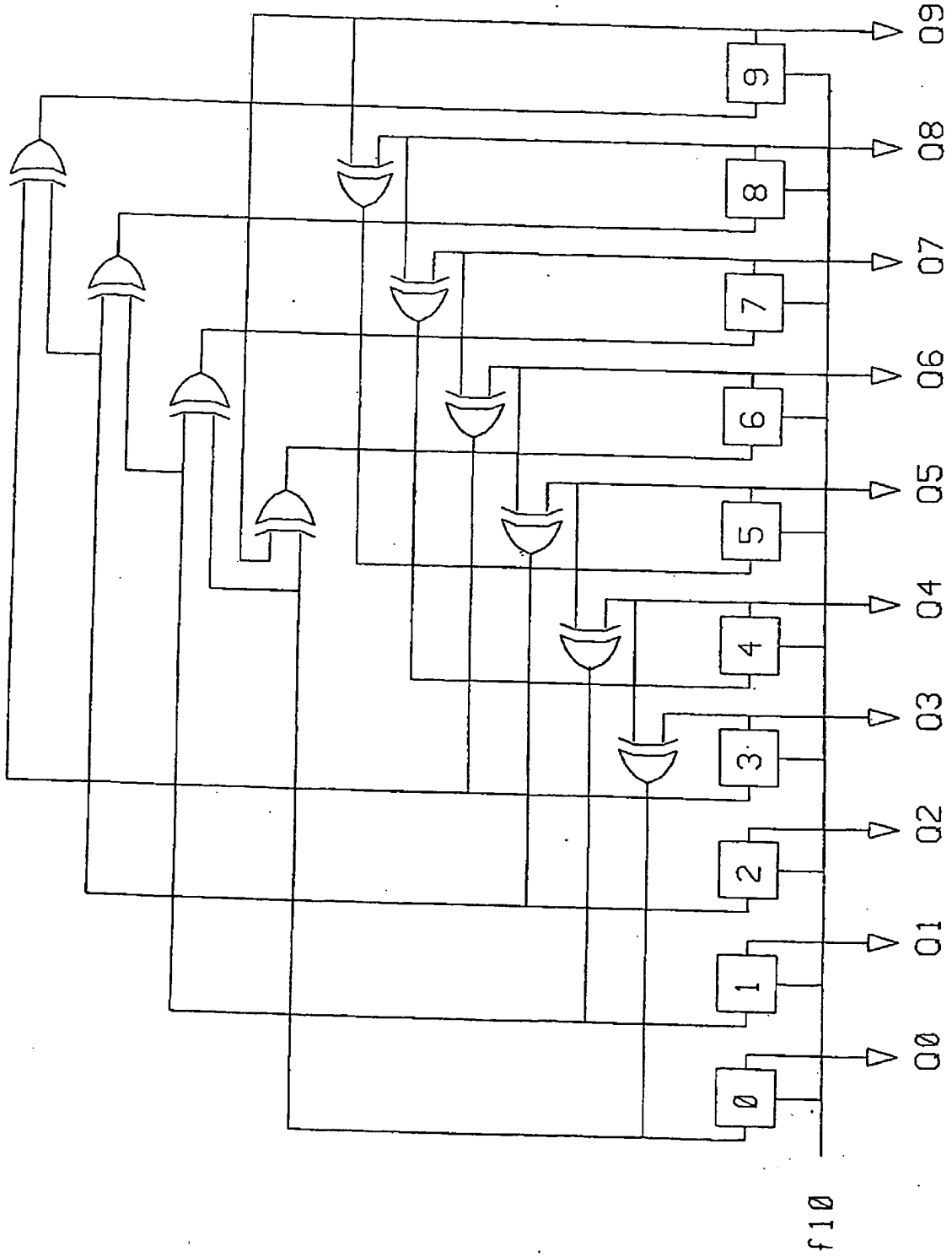

Figure 3A

the equations are:

$$D0(n) = Q3(n-1) \oplus Q4(n-1)$$
$$D1(n) = Q4(n-1) \oplus Q5(n-1)$$
$$D2(n) = Q5(n-1) \oplus Q6(n-1)$$
$$D3(n) = Q6(n-1) \oplus Q7(n-1)$$
$$D4(n) = Q7(n-1) \oplus Q8(n-1)$$
$$D5(n) = Q8(n-1) \oplus Q9(n-1)$$
$$D6(n) = Q9(n-1) \oplus D\phi(n)$$
$$D7(n) = D0(n) \oplus D1(n)$$
$$D8(n) = D1(n) \oplus D2(n)$$
$$D9(n) = D2(n) \oplus D3(n)$$

table 1: state equations for schematic shown in figure 3

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